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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,095	03/30/2001	Koichi Hashimoto	740250-837	2229
22204	7590	11/16/2004	EXAMINER	
NIXON PEABODY, LLP 401 9TH STREET, NW SUITE 900 WASHINGTON, DC 20004-2128			DIVINE, LUCAS	
			ART UNIT	PAPER NUMBER
			2624	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/821,095

**Applicant(s)**

HASHIMOTO ET AL.

**Examiner**

Lucas Divine

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2001.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities: print section does not have a **6** after it in page 26 line 16. Appropriate correction is required.

### *Claim Objections*

2. Claim 2 is objected to because of the following informalities: page 51 line 23 states the phrase '**cycle cycle**'. Appropriate correction to remove the redundant word is required.
3. Claim 5 is objected to because of the following informalities: page 52 line 19: '**Further,**' should be '*further comprising:*'.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 5, which depends from claim 1, on page 52 lines 24-26, claim 5 recites '**to transfer the same** (input data that would have been going into the mounted module) **to a component rearward of the signal processor when it is not mounted**'. This limitation is not

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described in the specification because the specification describes transferring the same to a component **forward** of the signal processor when it is not mounted. In the specification, page 14, lines 6 – 20 discuss the transfer modes for when a DSP module is mounted in the system and when it is not. In the given example, applicant states ‘**whereas the second stage DSP module DSP1 is not mounted on the circuit board, the first stage DSP module DSP0 input data into the data input port DI of the third stage DSP module DSP2 through the short circuiting terminals J1**’. Thus, when a DSP module, according to the disclosure, is removed from the system, the data that would have been inputted to it is thus transferred to the component **forward** of the removed module. Therefore, claim 5 is rejected for not providing written description of claimed elements.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Lyons (US 5903574).

Regarding claim 1, Lyons teaches **an image processing apparatus comprising at least two signal processor modules interconnected each other in series** (Fig. 2 modules 132 and 136 connected in series through a communication channel 134), **each of the signal processor**

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**modules having an input port through which data is input** (input ports by step S6 to module 132 and 136C for module 136), **a memory which stores data** (the operations involved in decoding and encoding inherently include some sort of memory to complete the operation on large portions of data over a period of time, e.g. registers, RAM), **a signal processor portion which carries out processing on input data according to program** (processing completed in 132B and 136B) **and an output port through which data is output** (output of module 132 by S7 and of module 136 by S9, both in Fig. 2), **wherein the improvement comprises**

**that at least one of the signal processor modules outputs both unprocessed input data and processed data obtained by processing the input data** (col. 3 lines 40-42 discuss module 136 having the ability to output both unprocessed or processed data).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lyons in view of Ahamed et al. (US 5978831) hereafter referred to as Ahamed.

Regarding claim 2, which depends from claim 1, Lyons teaches all of the limitations of parent claim 1.

Lyons further teaches

**said at least one of the signal processor modules 136:**

**stores unprocessed input data as input through the input port** (decoder 136 implicitly stores the unprocessed data from the input 136C in order to perform the output of unprocessed data; col. 3 line 43) **and processed data obtained by reading out and processing unprocessed input data stored in the memory** (decoder 136 implicitly stores the processed data output by decoder 136B in order to perform the output of processed data; col. 3 line 42) **and**

**outputs through the output port unprocessed data and processed data stored in the memory** (col. 3 lines 40-43 teaches the outputting of unprocessed data and processed data stored in the decoder 136), **and**

**the other signal processor module(s) 132:**

**stores in the memory unprocessed input data as input through the input port** (encoder 132 implicitly stores unprocessed data in order to perform processing on it as discussed in the rejection of claim 1) **and processed data obtained by reading out and processing unprocessed input data stored in the memory** (encoder 132 implicitly stores processed data and processes the data by reading from the implicit memory, processing, and writing back to memory as standard processing technique known to those of ordinary skill in the art; processing discussed in col. 3 lines 31-36) **and**

**outputs through the output port processed data stored in the memory** (Fig. 2 by S7, encoder module 132 outputs encoded 'processed' data).

While Lyons teaches processor modules receiving, processing, and outputting data, Lyons does not specifically teach the **input, processing, and output as being controlled synchronously within cycles.**

Ahamed teaches the **input, processing, and output as being controlled synchronously within cycles** (Fig. 7 clock 21 which controls the data transfers of the processors by the unit of clock cycles).

It would have been obvious to add the synchronous behavior of Ahamed to the system of Lyons. The motivation for doing so would have been to coordinate data transfers between modules of differing processing speeds better than asynchronously (col. 3 lines 3-8). Other advantages of synchronous – clock driven – processor modules are well known in the art.

Regarding claim 3, which depends from claim 2 as it depends from claim 1, Ahamed further teaches **a synchronous circuit which causes data transfer for signal processor modules to occur in synchronization with clocks which are the same in phase and frequency** (Fig. 7 clk 21 causes data transfers for processor modules 11 and 12).

Regarding claim 4, which depends from claim 3 as it depends from claims 1 and 2,

Lyons further teaches **the data transfer widths between the signal processor modules are equal to each other** (in Fig. 2, Lyons suggests that the data transfer widths between modules are equal to each other by assigning the same type, shape, and size of line on the output of module 132 – by S7 – and on the input of module 136 – by S8) **and**

Ahamed further teaches **the synchronous circuit determines the frequency of the transfer clock on the basis of the data transfer rate between the pair of signal processor modules between which the largest amount of data is to be transferred** (Ahmed teaches the determination of clk frequency based on the data transfer rate of the slow processor 11; by adding the synchronization features of Ahamed to the module transfers of Lyons as discussed in the rejection of claim 2, the determination of the clock frequency would be based on the speeds

of the processor modules 132 and 136 and the amount of data between them, which would have been obvious to one of ordinary skill in the art).

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lyons and Durkos et al. (US 4777590) hereafter referred to as Durkos.

Regarding claim 5, which depends from claim 1, Lyons teaches all of the limitations of claim parent claim 1 as discussed above.

While Lyons teaches a system with multiple functional modules for performing computing tasks, Lyons does not specifically teach **a mounting means on which a signal processor module is removably mounted is provided for at least one of the signal processor modules and a switching means is provided for said at least one signal processor module to transfer data to the signal processor module through its input port when it is mounted on the mounting means and to transfer the same to a component rearward of the signal processor module when it is not mounted on the mounting means.**

Durkos teaches a system with multiple functional modules for performing computing tasks including:

**a mounting means on which a signal processor module is removably mounted is provided for at least one of the signal processor modules** (Fig. 4, wherein the modules 102 can be removably plugged-in 'mounted' in the system) **and**

**a switching means is provided for said at least one signal processor module to transfer data to the signal processor module through its input port when it is mounted on the mounting means and to transfer the same to a component rearward of the signal**



**processor module when it is not mounted on the mounting means** (Fig. 4, wherein module select circuit 56 acts as a switching means by switching which plugged-in 'mounted' modules 102 are connected to each other in the system, and when a module is not plugged-in to the system, data is routed to the next module).

It would have been obvious to one of ordinary skill in the art to provide a system with the modules of Lyons that are mountable as in Durkos. Durkos teaches that the modules are in series (wherein the block arrows between modules signify connections in Fig. 4) and teaches modules with different functionalities. It would have been obvious to one of ordinary skill that a module in Durkos could have been an encoding or decoding module such as in Lyons. The motivations for doing so would have been to provide for an easily customizable and upgradeable system (Durkos col. 1 lines 51-52).

### *Conclusion*

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US-6366951, Schmidt, 4/2/2002: teaches a distributed processing system including a switching means for switching the routing between computing modules.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucas Divine whose telephone number is 703-306-3440. The examiner can normally be reached on Monday - Friday, 7:30am - 5:00pm.

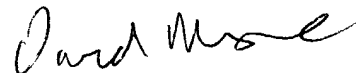
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached on 703-308-7452. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lucas Divine  
Examiner  
Art Unit 2624

ljd



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**SUPERVISORY PATENT EXAMINER**  
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